FIG.1

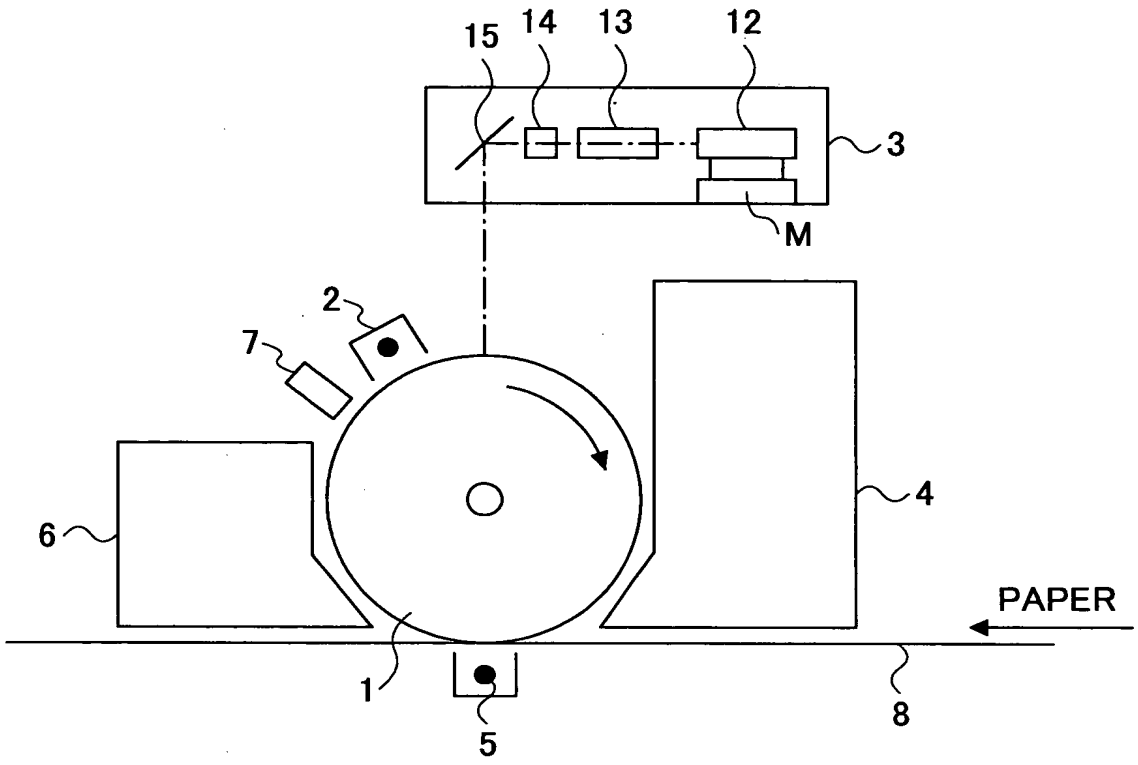


FIG.2

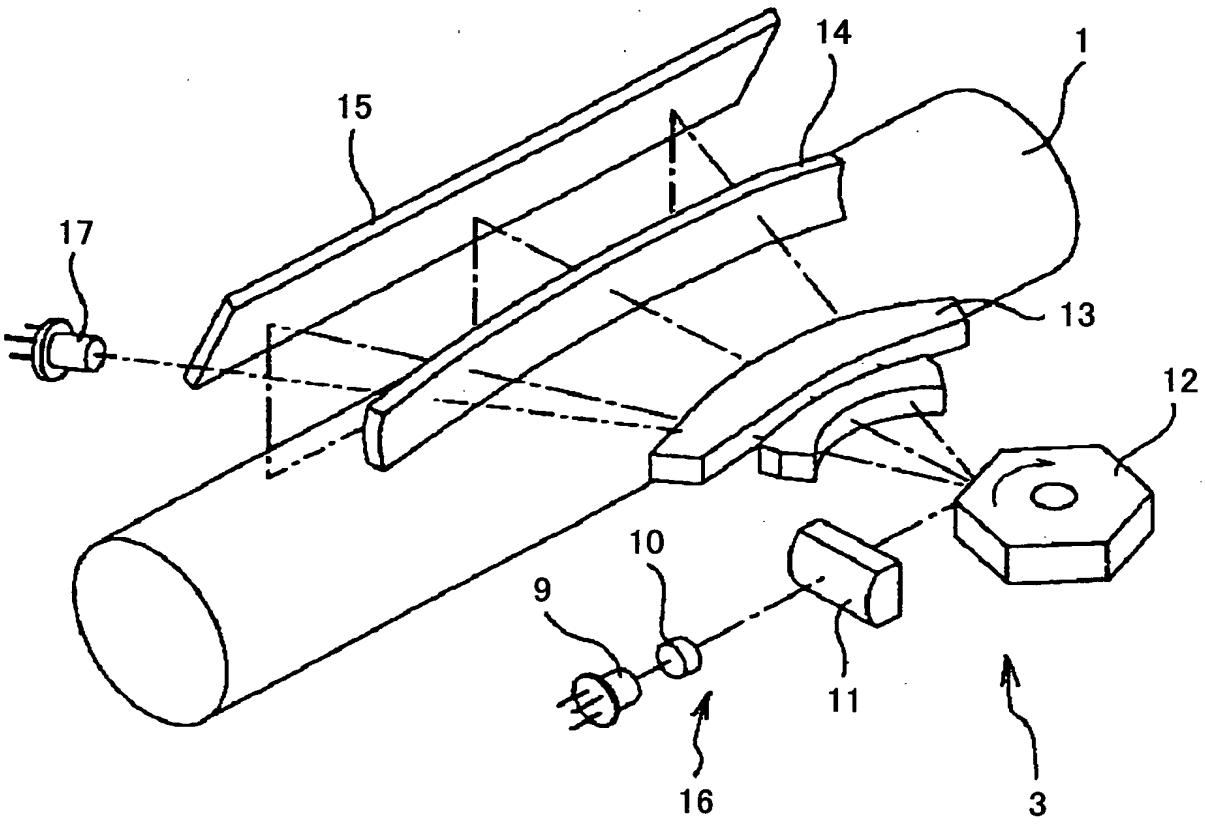


FIG.3

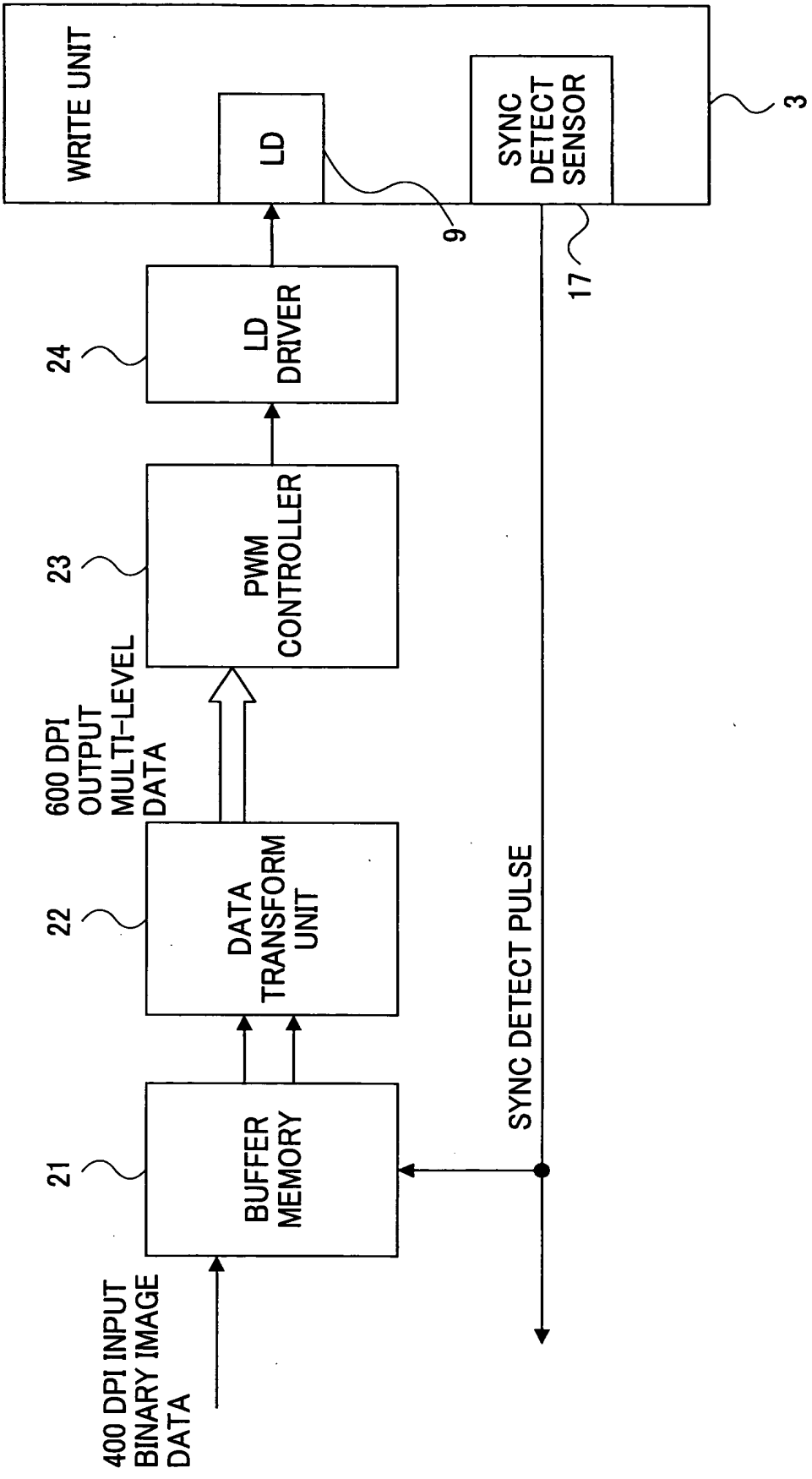

WRITE UNIT
LD
SYNC DETECT SENSOR
3
9
17
24
LD DRIVER
23
PWM CONTROLLER
600 DPI OUTPUT MULTI-LEVEL DATA
22
DATA TRANSFORM UNIT
SYNC DETECT PULSE
21
BUFFER MEMORY
400 DPI INPUT BINARY IMAGE DATA

FIG.4

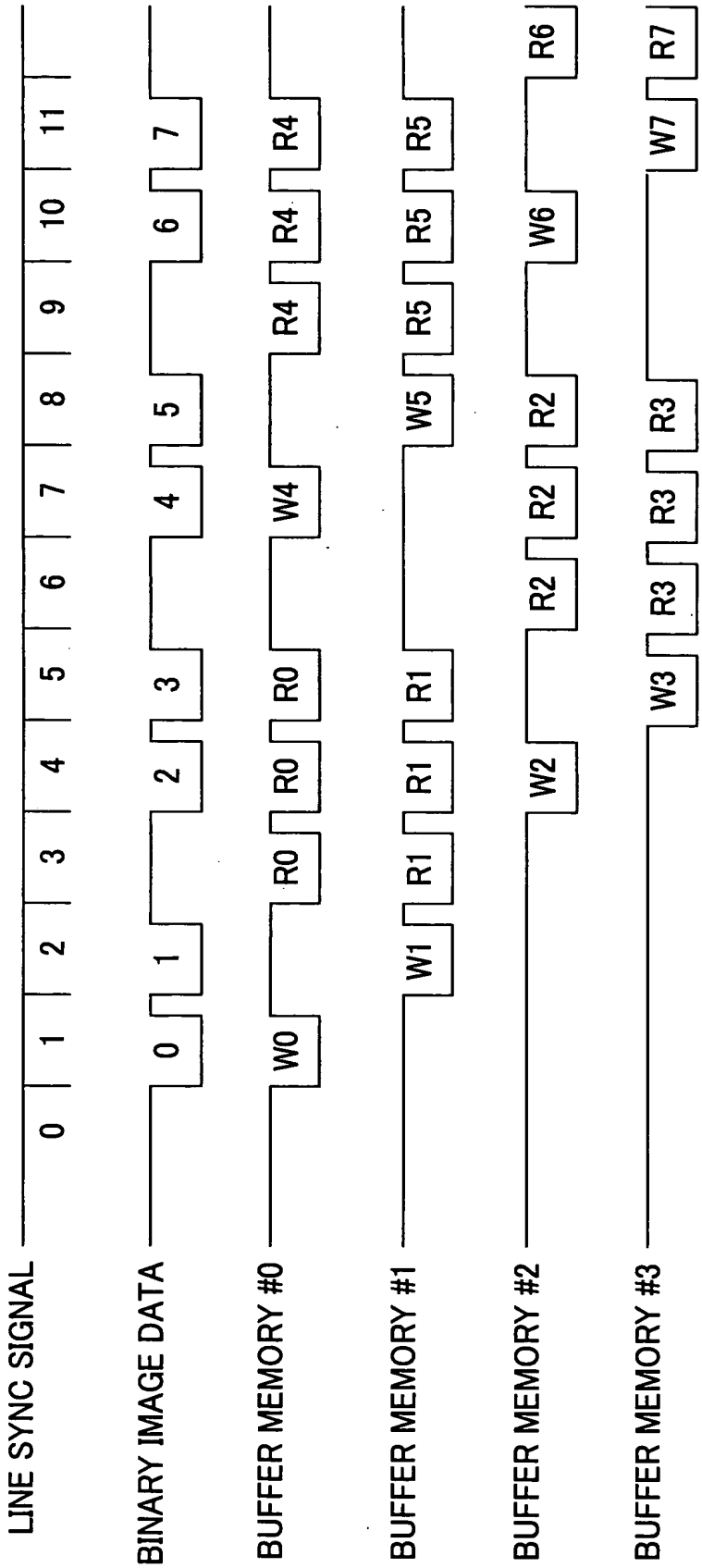
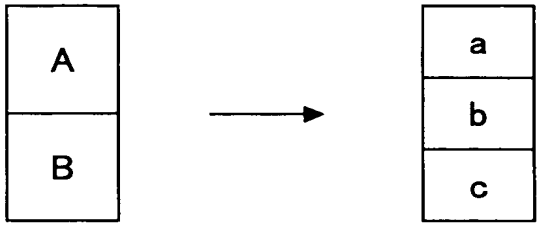
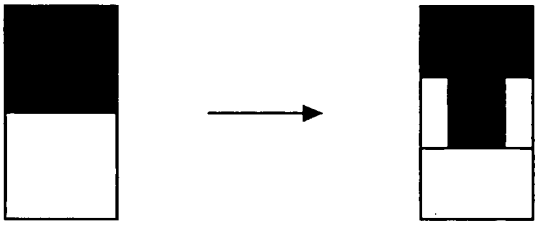

LINE SYNC SIGNAL
0 1 2 3 4 5 6 7 8 9 10 11
INPUT BINARY IMAGE DATA
0 1 2 3 4 5 6 7
BUFFER MEMORY #0
W0 R0 R0 R0 W4 R4 R4 R4
BUFFER MEMORY #1
W1 R1 R1 R1 W5 R5 R5 R5
BUFFER MEMORY #2
W2 R2 R2 R2 W6 R6
BUFFER MEMORY #3
W3 R3 R3 R3 W7 R7

FIG.5



400dpi MAIN 400 DPI X SUB 600 DPI

FIG.6



400dpi MAIN 400 DPI X SUB 600 DPI

BEST AVAILABLE COPY

FIG.7

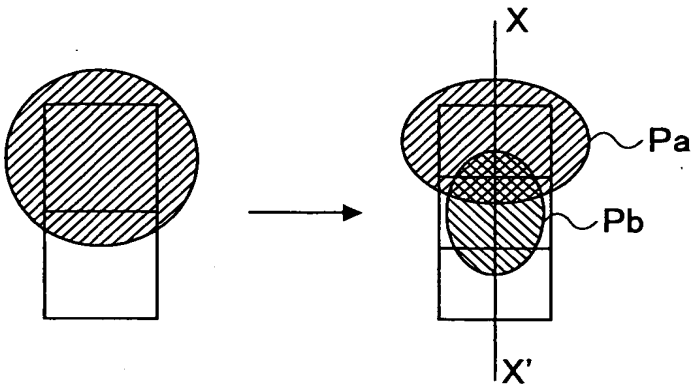


FIG.8

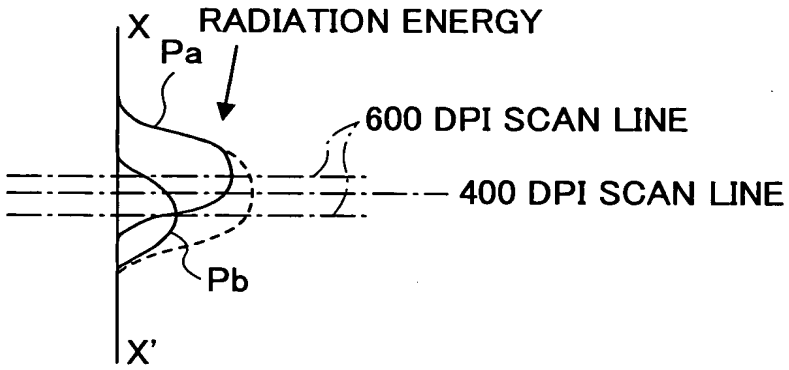


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FIG.9

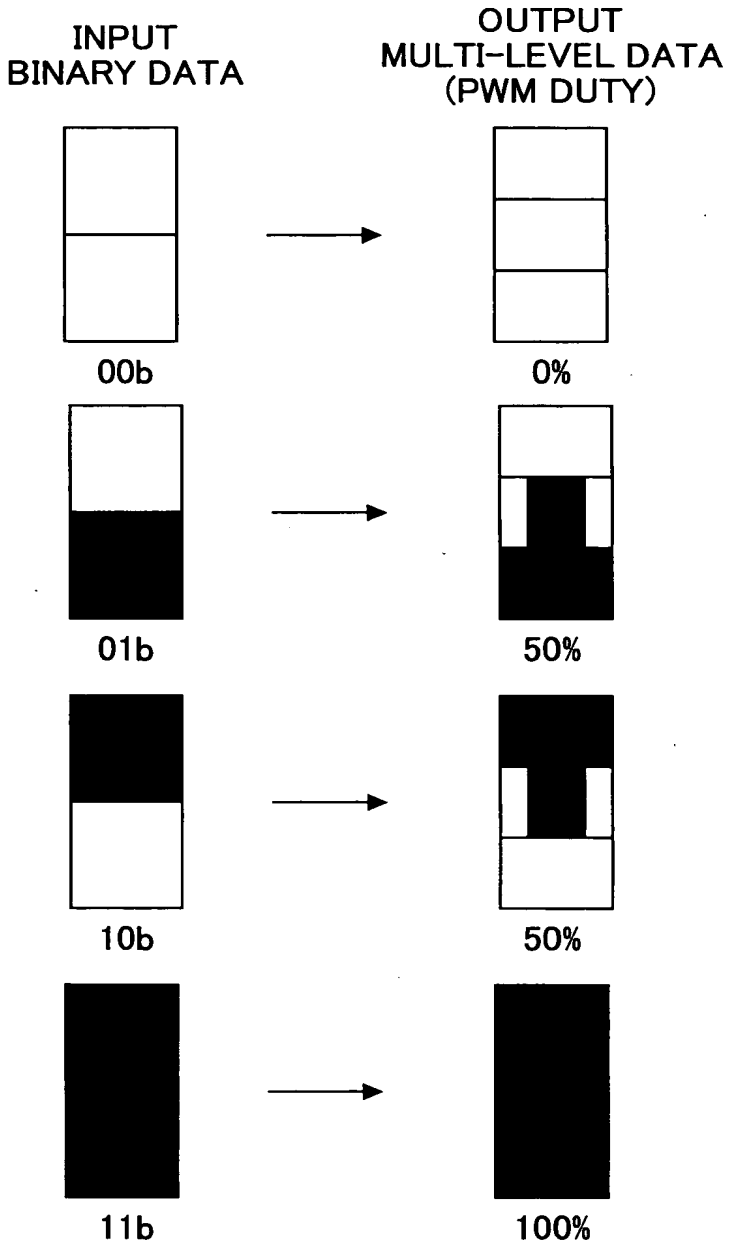

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FIG.10A

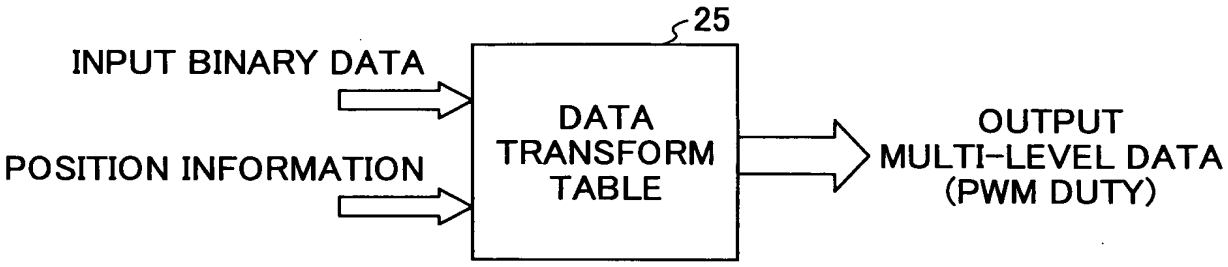

FIG.10B

INPUT BINARY DATA AB	POSITION INFORMATION	OUTPUT MULTI-LEVEL DATA (PWM DUTY)
≀	≀	≀
10	a b c	100% 50% 0%
≀	≀	≀

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FIG.11

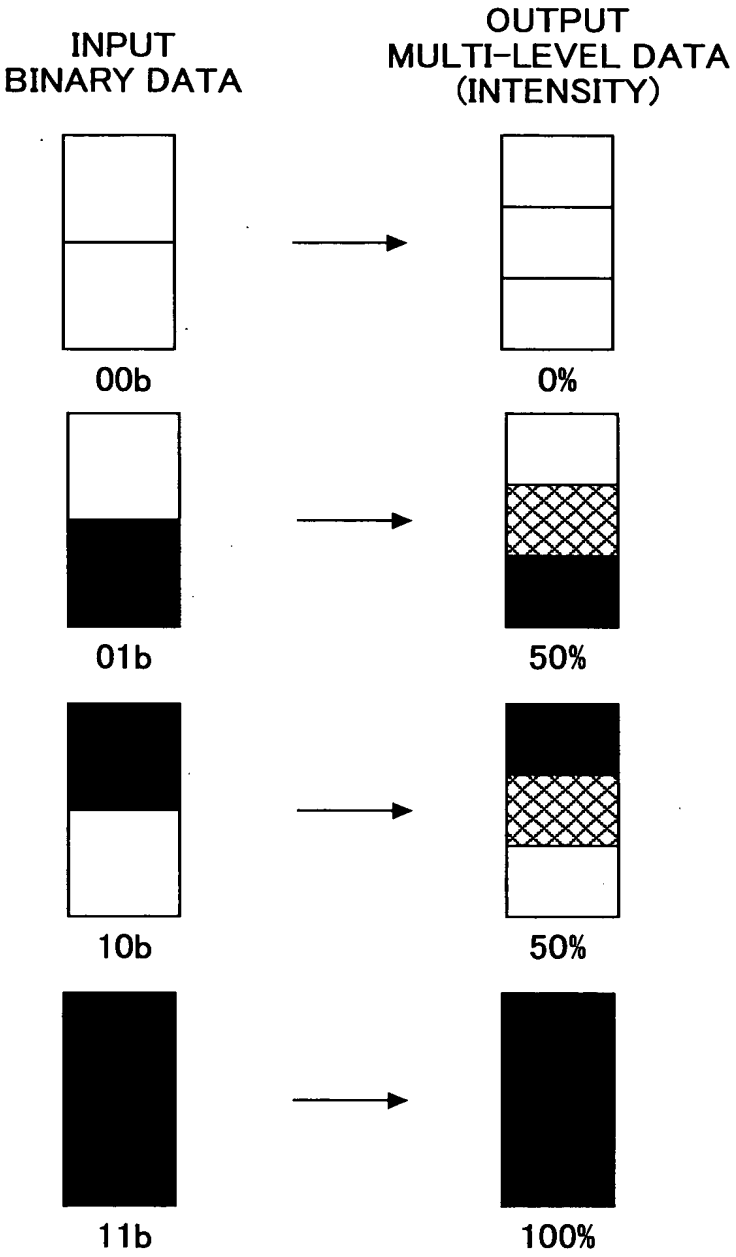

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FIG.12

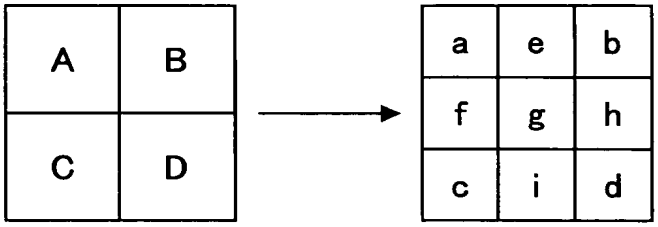


FIG.13

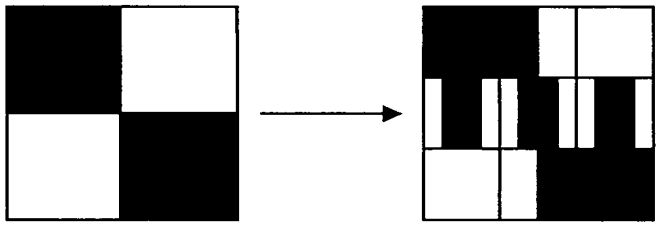
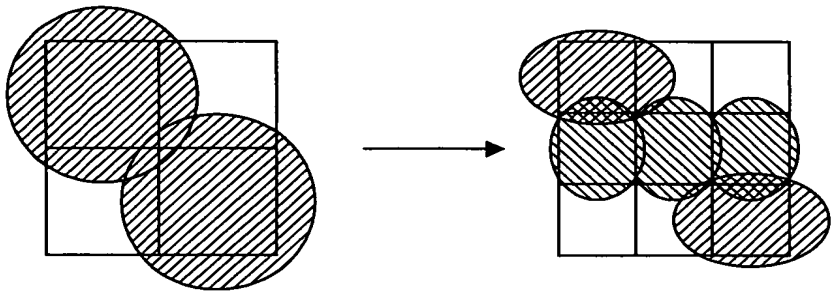
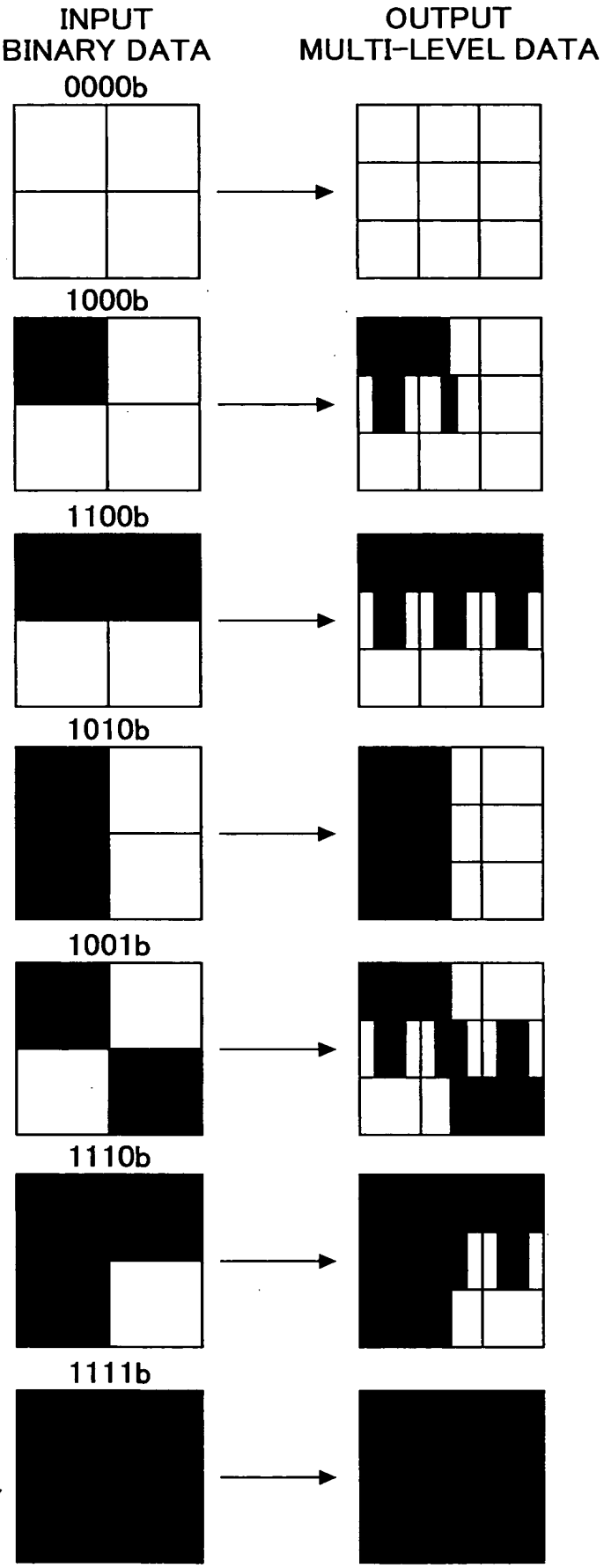


FIG.14



BEST AVAILABLE COPY

FIG.15



BEST AVAILABLE COPY

FIG.16A

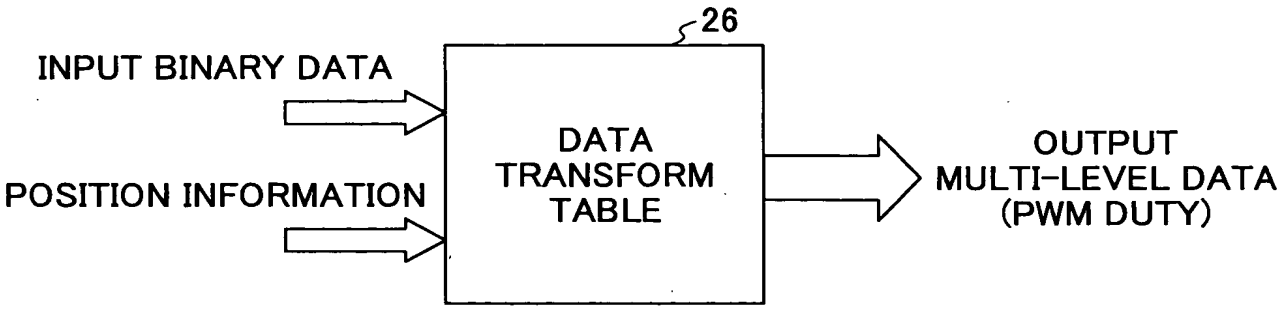


FIG.16B

INPUT BINARY DATA ABCD	POSITION INFORMATION	OUTPUT MULTI-LEVEL DATA (PWM DUTY)	PHASE
≀	≀	≀	≀
1110	a b c d e f g h i	100% 100% 100% 0% 100% 100% 75% 50% 50%	— — — — 0 — −1 — −1
≀	≀	≀	≀

BEST AVAILABLE COPY

FIG.17

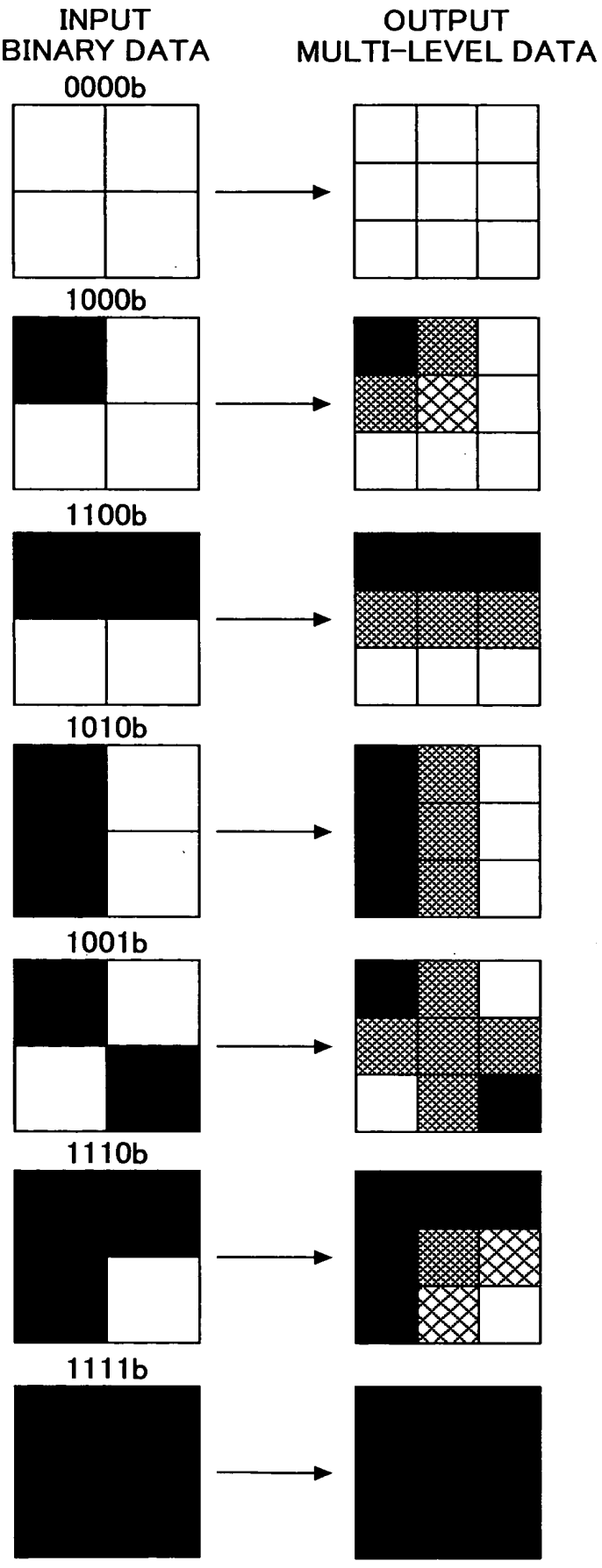


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FIG.18

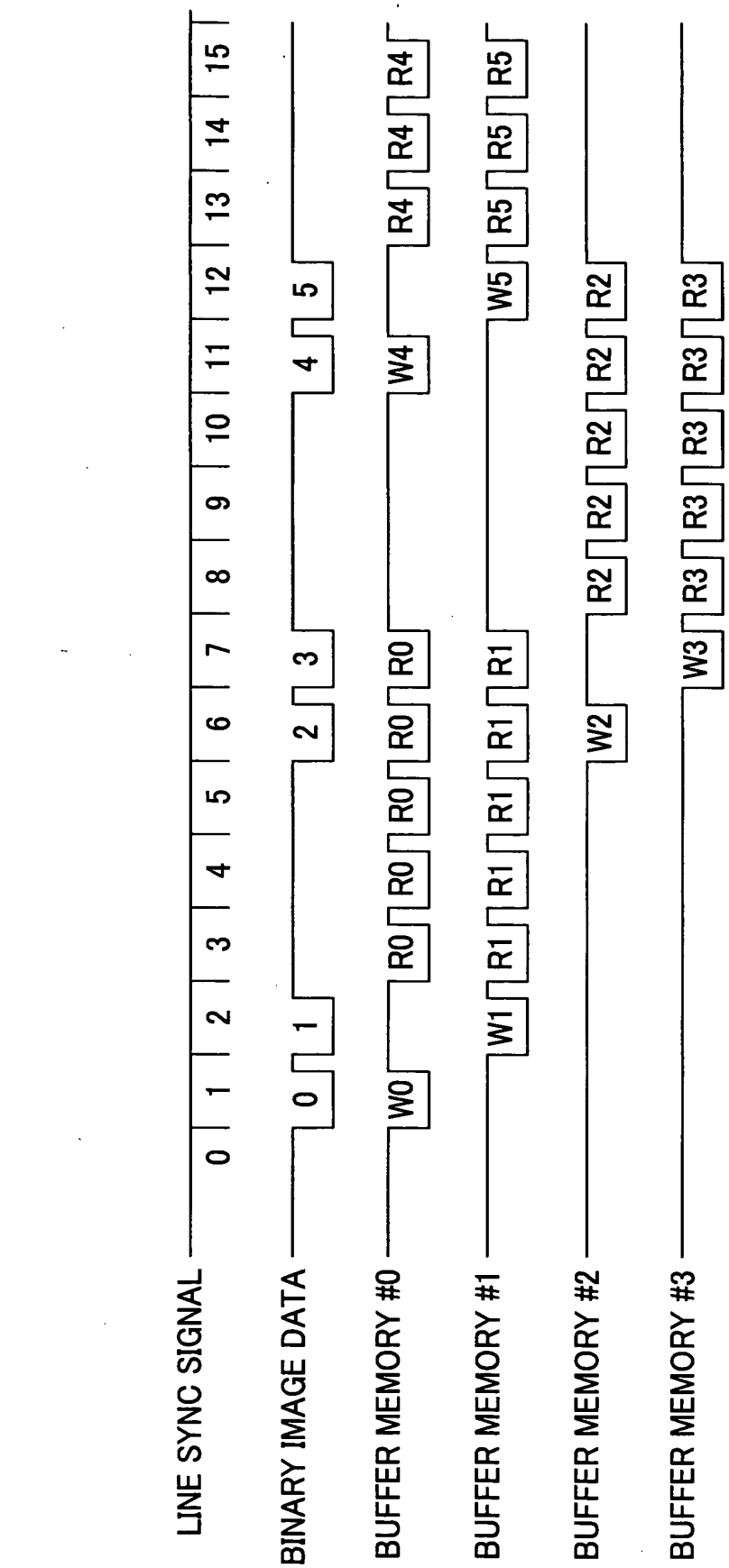
LINE SYNC SIGNAL
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
INPUT BINARY IMAGE DATA
0 1 2 3 4 5
BUFFER MEMORY #0
W0 R0 R0 R0 R0 R0 W4 R4 R4 R4
BUFFER MEMORY #1
W1 R1 R1 R1 R1 R1 W5 R5 R5 R5
BUFFER MEMORY #2
W2 R2 R2 R2 R2 R2
BUFFER MEMORY #3
W3 R3 R3 R3 R3 R3

FIG.19

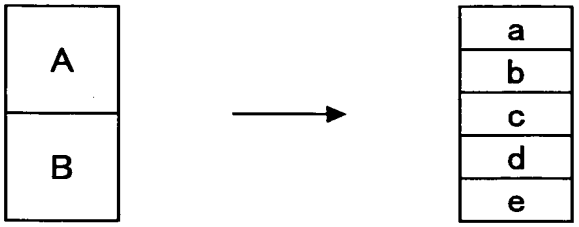

FIG.20

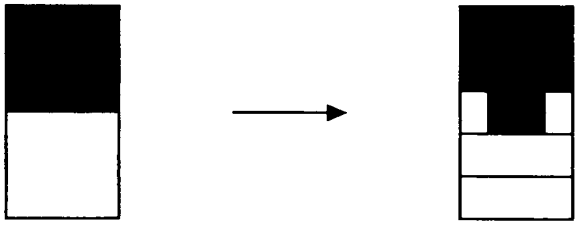

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FIG.21

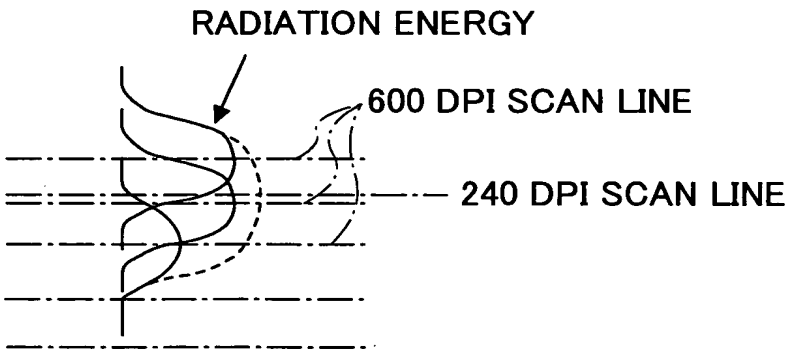

FIG.22

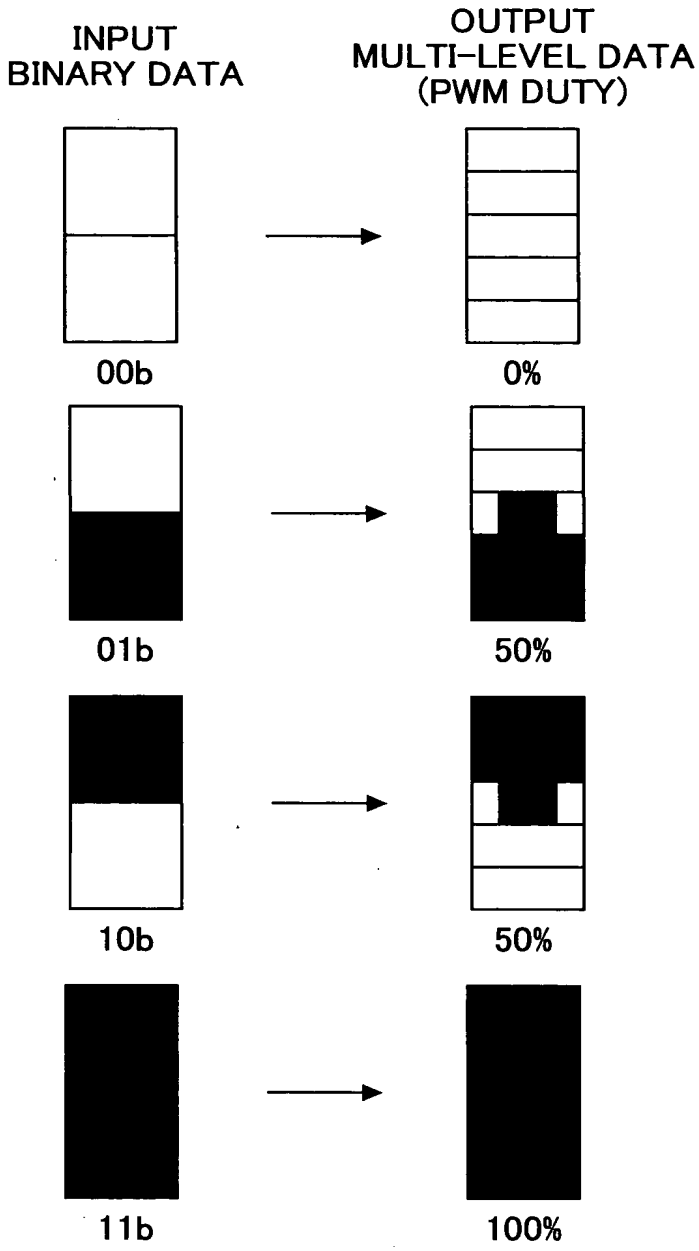

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FIG.23

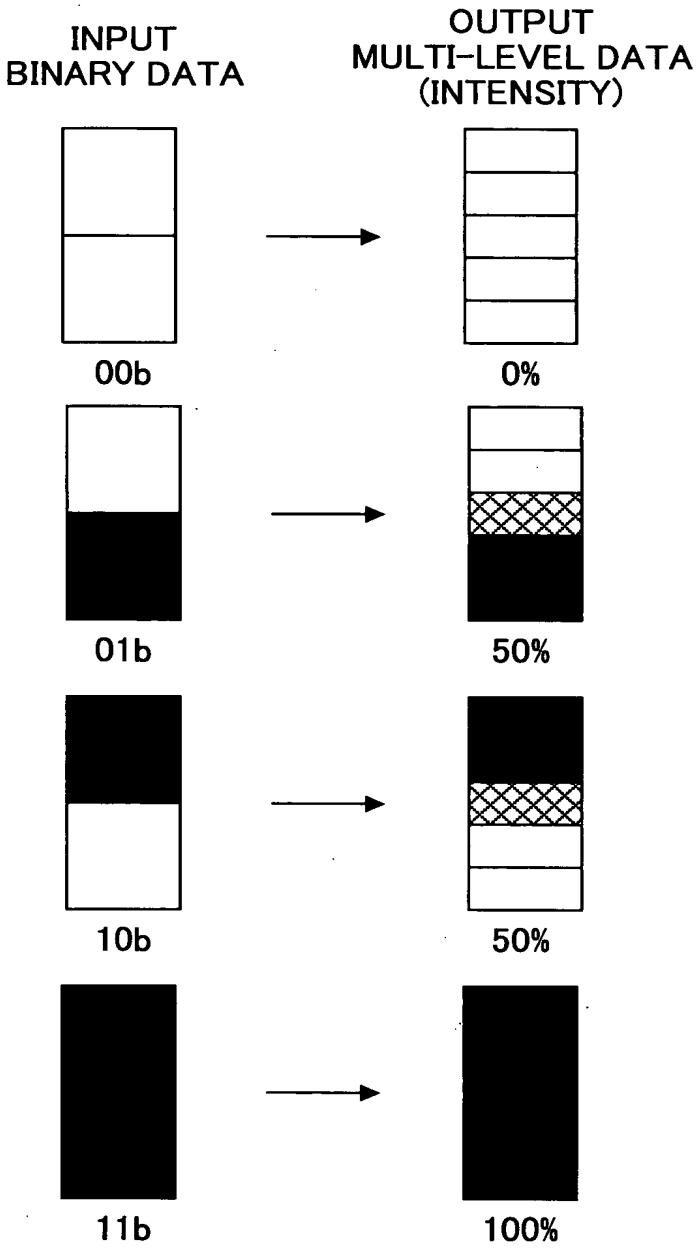

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FIG.24

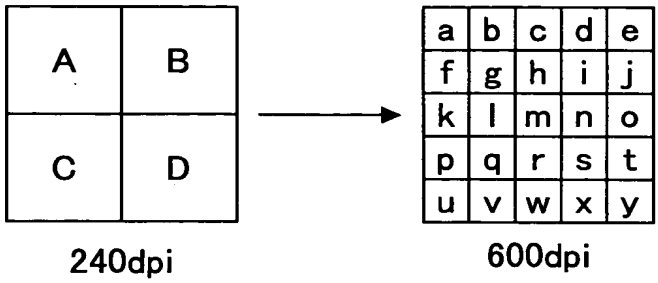

FIG.25

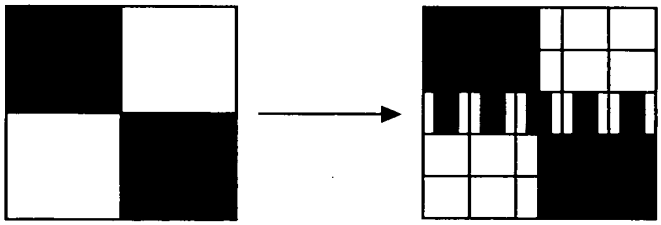

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FIG.26

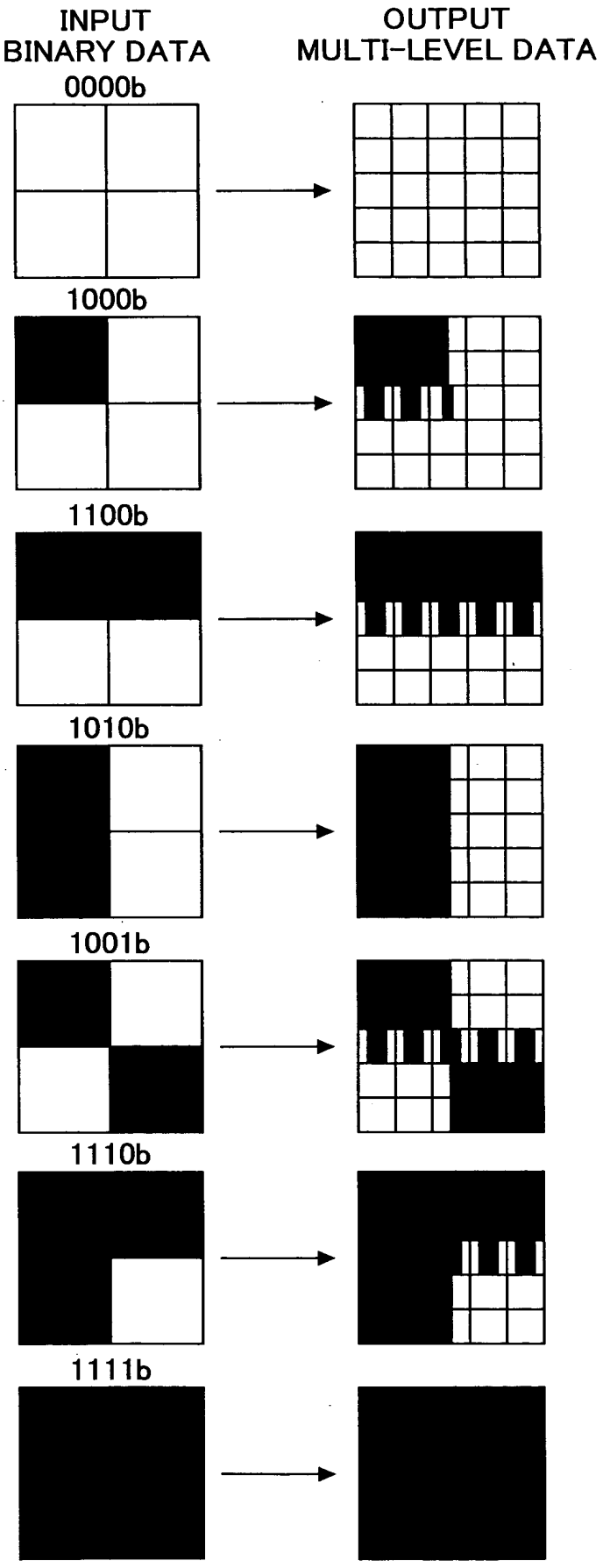

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FIG.27

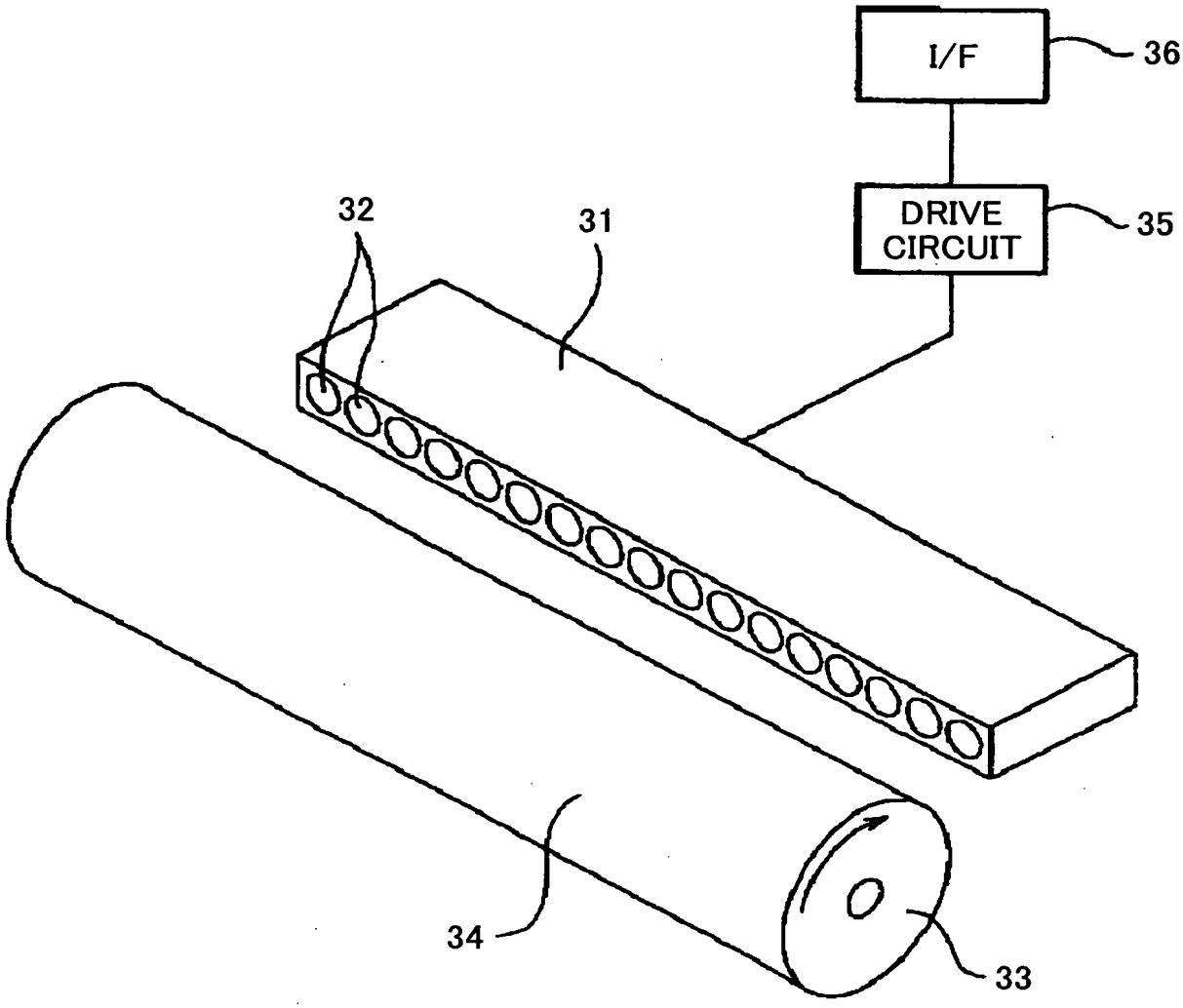

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FIG.28

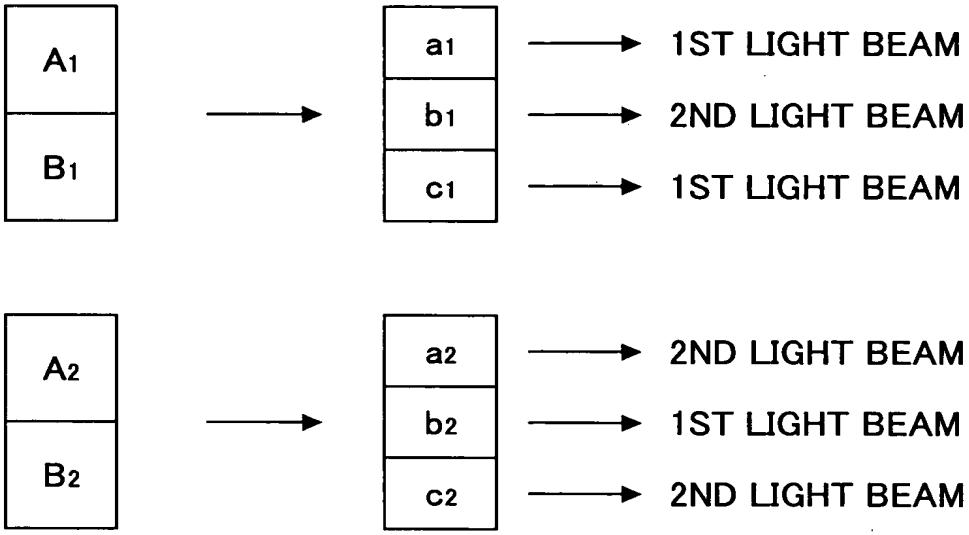
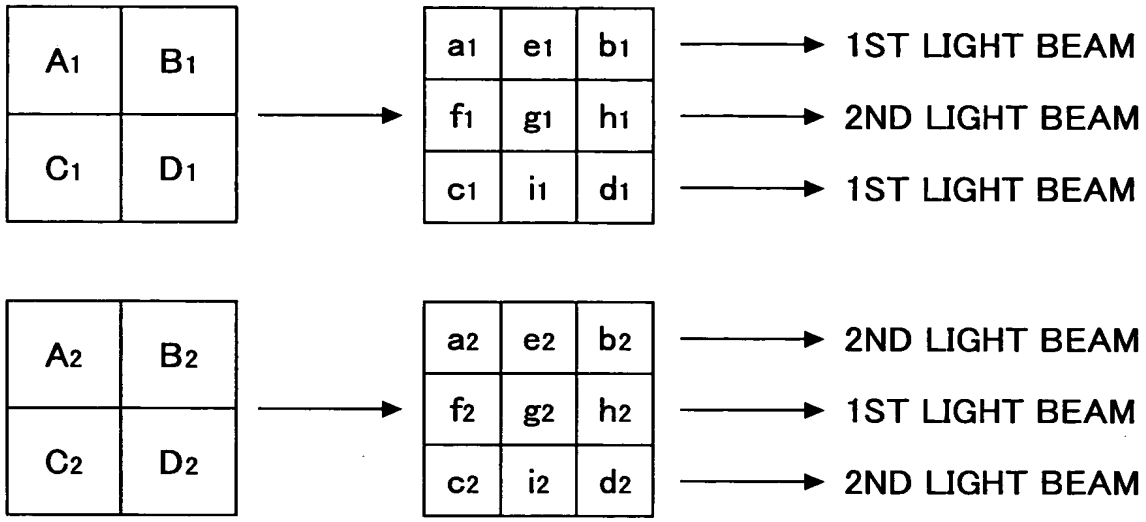

A1
B1
a1
b1
c1
1ST LIGHT BEAM
2ND LIGHT BEAM
1ST LIGHT BEAM
A2
B2
a2
b2
c2
2ND LIGHT BEAM
1ST LIGHT BEAM
2ND LIGHT BEAM

FIG.29


A1
B1
C1
D1
a1
e1
b1
f1
g1
h1
c1
i1
d1
1ST LIGHT BEAM
2ND LIGHT BEAM
1ST LIGHT BEAM
A2
B2
C2
D2
a2
e2
b2
f2
g2
h2
c2
i2
d2
2ND LIGHT BEAM
1ST LIGHT BEAM
2ND LIGHT BEAM